1. A booting circuit connecting an external interface to an internal line of a device, the line being adapted to supply a programming voltage to a programmable element in the device during a programming operation, said booting circuit comprising:

a precharge circuit having a precharge output responsive to a plurality of control signals;

a clamping circuit responsive to said control signals and being adapted to receive the programming voltage from the line, said clamping circuit outputting a clamped programming voltage when activated by said control signals;

a first circuit connected to the line and said clamping circuit, said first circuit having a first output having a first voltage level based on the programming voltage or a second voltage level based on the clamped programming voltage; and

a bootable element connected between the external interface and the internal line, said bootable element being controlled by said precharge output and the first output to allow the programming voltage to be directly applied to the line while preventing a full level of the programming voltage from being sent to the external interface during a first programming mode.

2. The booting circuit of claim 1, wherein said clamping circuit comprises a voltage divider circuit that is activated when said control signals are indicative of the first programming mode.

3. The booting circuit of claim 1, wherein clamping circuit comprises:

an inverter adapted to receive a first control signal, said inverter having a second output;

a NAND gate adapted to receive a second control signal and said second output, said NAND gate having a third output;

a first switchable element connected to said third output; and

a plurality of resistive elements connected between said third output and said line, wherein said resistive elements are switched into said clamping circuit when said control signals are indicative of the first programming mode.

4. The booting circuit of claim 3, wherein said resistive elements comprises diode-connected transistors.

5. The booting circuit of claim 1, wherein said bootable element is controlled by said precharge output and the first output to isolate the external interface from the line during normal operation of the device.

6. The booting circuit of claim 5, wherein said precharge output is a ground potential when said control signals are indicative of a normal operating mode of the device.

7. The booting circuit of claim 1, wherein said bootable element is controlled by said precharge output and the first output to pass an externally supplied program voltage from the external interface to the line during a second programming mode of the device.

8. The booting circuit of claim 7, wherein said precharge output is a pumped potential when said control signals are indicative of the second programming mode.

9. The booting circuit of claim 7, wherein said first output is said first level when said control signals are indicative of the second programming mode.

10. The booting circuit of claim 1, wherein said precharge output is a pumped potential when said control signals are indicative of a programming mode of the device.

11. The booting circuit of claim 1, wherein said first output is said second level when said control signals are indicative of the first programming mode.

12. The booting circuit of claim 1, wherein said bootable element is a transistor.

13. The booting circuit of claim 1, wherein said first circuit comprises a booting capacitor circuit.

14. A memory device comprising:

an external interface;

a signal line adapted to supply a programming voltage to a programmable element in said device;

a booting circuit connected between said external interface and said signal line, said booting circuit comprising:

a precharge circuit having a precharge output responsive to first and second control signals;

a clamping circuit responsive to said control signals and being adapted to receive the programming voltage from said signal line, said clamping circuit outputting a clamped programming voltage when activated by said control signals;

a first circuit connected to said signal line and said clamping circuit, said first circuit having a first output based on the programming voltage or the clamped programming voltage; and

a bootable element connected between said external interface and said signal line, said bootable element being controlled by said precharge output and said first output to allow the programming voltage to be directly applied to said signal line while preventing a full level of the programming voltage from being passed to said external interface during a first programming mode.

15. The memory device of claim 14, wherein said clamping circuit comprises a voltage divider circuit that is activated when said control signals are indicative of the first programming mode.

16. The memory device of claim 14, wherein clamping circuit comprises:

an inverter adapted to receive a first control signal, said inverter having a second output;

a NAND gate adapted to receive a second control signal and said second output, said NAND gate having a third output;

a first switchable element connected to said third output; and

a plurality of resistive elements connected between said third output and said signal line, wherein said resistive elements are switched into said clamping circuit when said control signals are indicative of the first programming mode.

17. The memory device of claim 16, wherein said resistive elements comprises diode-connected transistors.

18. The memory device of claim 14, wherein said bootable element is controlled by said precharge output and the first output to isolate said external interface from said signal line during normal operation of said memory device.

19. The memory device of claim 18, wherein said precharge output is a ground potential when said control signals are indicative of a normal operating mode of said memory device.

20. The memory device of claim 14, wherein said bootable element is controlled by said precharge output and the first output to pass an externally supplied program voltage from said external interface to said signal line during a second programming mode of said memory device.

21. The memory device of claim 20, wherein said precharge output is a pumped potential when said control signals are indicative of the second programming mode.

22. The memory device of claim 14, wherein said precharge output is a pumped potential when said control signals are indicative of a programming mode of said memory device.

23. The memory device of claim 14, wherein said bootable element is a transistor.

24. The memory device of claim 14, wherein said first circuit comprises a booting capacitor circuit.

25. The memory device of claim 14, wherein said external interface is a bond pad.

26. A memory device comprising:

an external programming pin;

an internal line that is programmable by a voltage received from said external programming pin and by a voltage received from another source; and

a booting circuit for selectively coupling said external programming pin with said internal line to allow said internal line to be programmed by a first voltage received by said external programming pin and for uncoupling said external programming pin from said internal line to allow said internal line to be programmed with a second voltage from said another source, said booting circuit ensuring that said internal line is programmed with a full voltage level of said first and second voltages.

27. The memory device of claim 26, wherein said booting circuit comprises a clamping circuit for limiting a level of said second voltage as applied to said external programming pin.

28. The memory device of claim 27, wherein said clamping circuit is activated during a first programming mode of said memory device.

29. The memory device of claim 28, wherein said booting circuit allows said internal line to be programmed by said first voltage during a second programming mode of said memory device.

30. The memory device of claim 27, wherein said clamping circuit comprises a voltage divider circuit.

31. A processor system comprising:

a processor; and

a memory device coupled to said processor, said memory device comprising an external interface, a signal line adapted to supply a programming voltage to a programmable element in said device, and a booting circuit connected between said external interface and said signal line, said booting circuit comprising:

a precharge circuit having a precharge output responsive to first and second control signals;

a clamping circuit responsive to said control signals and being adapted to receive the programming voltage from said signal line, said clamping

circuit outputting a clamped programming voltage when activated by said control signals;

a first circuit connected to said signal line and said clamping circuit, said first circuit having a first output based on the programming voltage or the clamped programming voltage; and

a bootable element connected between said external interface and said signal line, said bootable element being controlled by said precharge output and said first output to allow the programming voltage to be directly applied to said signal line while preventing a full level of the programming voltage from reaching said external interface during a first programming mode.

32. The system of claim 31, wherein said clamping circuit comprises a voltage divider circuit that is activated when said control signals are indicative of the first programming mode.

33. The system of claim 31, wherein clamping circuit comprises:

an inverter adapted to receive a first control signal, said inverter having a second output;

a NAND gate adapted to receive a second control signal and said second output, said NAND gate having a third output;

a first switchable element connected to said third output; and

a plurality of resistive elements connected between said third output and said signal line, wherein said resistive elements are switched into said clamping circuit when said control signals are indicative of the first programming mode.

34. The system of claim 33, wherein said resistive elements comprises diode-connected transistors.

35. The system of claim 31, wherein said bootable element is controlled by said precharge output and the first output to isolate said external interface from said signal line during normal operation of said memory device.

36. The system of claim 35, wherein said precharge output is a ground potential when said control signals are indicative of a normal operating mode of said memory device.

37. The system of claim 31, wherein said bootable element is controlled by said precharge output and the first output to pass an externally supplied program voltage from said external interface to said signal line during a second programming mode of said memory device.

38. The system of claim 37, wherein said precharge output is a pumped potential when said control signals are indicative of the second programming mode.

39. The system of claim 31, wherein said precharge output is a pumped potential when said control signals are indicative of a programming mode of said memory device.

40. The system of claim 31, wherein said bootable element is a transistor.

41. The system of claim 31, wherein said first circuit comprises a booting capacitor circuit.

42. The system of claim 31, wherein said external interface is a bond pad.

43. A processor system comprising:

a processor; and

a memory device coupled to said processor, said memory device comprising:

an external programming pin,

an internal line that is programmable by a voltage received from said external programming pin and by a voltage received from another source, and

a booting circuit for selectively coupling said external programming pin with said internal line to allow said internal line to be programmed by a first voltage received by said external programming pin and for uncoupling said external programming pin from said internal line to allow said internal line to be programmed with a second voltage from said another source, said booting circuit ensuring that said internal line is programmed with a full voltage level of said first and second voltages.

44. The system of claim 43, wherein said booting circuit comprises a clamping circuit for limiting a level of said second voltage as applied to said external programming pin.

45. The system of claim 44, wherein said clamping circuit is activated during a first programming mode of said memory device.

46. The system of claim 45, wherein said booting circuit allows said internal line to be programmed by said first voltage during a second programming mode of said memory device.

47. The system of claim 44, wherein said clamping circuit comprises a voltage divider circuit.

48. A method of programming a programmable element in a memory device, said method comprising the steps of:

inputting the programming voltage;

inputting control signals indicative of an operational mode of the memory device;

determining from said control signals whether the program voltage is being input from an external interface or from an internal signal line in the memory device; and

if it is determined that the program voltage is being input from the internal signal line, preventing the program voltage from being sent to the external interface while allowing the program voltage to reach the programmable element.

49. The method of claim 48, further comprising the step of passing the programming voltage to the signal line if it is determined that the program voltage is being input from the external interface.

50. The method of claim 49, wherein said step of inputting the programming voltage comprises inputting the programming voltage from a bond pad of the memory device.

51. The method of claim 48, wherein said step of inputting the programming voltage comprises inputting the programming voltage from a probe being applied directly to the signal line.